Claims

What is claimed is:

1. A method, comprising:

receiving an electrical idle ordered set at a receiving device power management unit;

entering a low power entry state if there is no activity on an interconnect when the electrical idle ordered set is received; and

bypassing the low power entry state and entering a low power reset state if there is activity on the interconnect when the electrical idle ordered set is received.

2. The method of claim 1, wherein entering a low power entry state includes turning off a receiver circuit in the receiving device.

3. The method of claim 2, further comprising entering a low power idle state following the low power entry state.

4. The method of claim 3, further comprising exiting the low power idle state and entering a low power receiver on state when activity is detected on the interconnect.

5. The method of claim 4, further comprising turning on the receiver circuit while in the low power receiver on state.

6. The method of claim 5, further comprising exiting the low power receiver on state and entering the low power receiver reset state.

7. An apparatus, comprising:

a receiver circuit to provide electrical connection to an interconnect;

an interconnect activity check unit coupled to the receiver circuit, the interconnect activity check unit to determine whether there is activity on the interconnect;

a pipeline to process incoming signals received at the receiver circuit; and

a power management unit to turn off the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit indicates that there is no activity on the interconnect, and the power management unit to not turn off the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit indicates that there is activity of the interconnect.

8. The apparatus of claim 7, wherein the pipeline includes a data extraction unit and a packet processing unit.

9. The apparatus of claim 8, the receiver circuit including a pair of inputs to receive a pair of differential signals, the differential signals included as part of the interconnect.

10. The apparatus of claim 9, the interconnect activity check unit to indicate that there is no activity on the interconnect if the differential pair of signals are at approximately a common mode voltage.

11. The apparatus of claim 10, the receiver circuit to provide electrical connection to a PCI Express interconnect.

12. A system, comprising:

a transmitting device; and

a receiving device coupled to the transmitting device via an interconnect, the receiving device including

a receiver circuit to provide electrical connection to the interconnect,

an interconnect activity check unit coupled to the receiver circuit, the interconnect activity check unit to determine whether there is activity on the interconnect,

a pipeline to process incoming signals received at the receiver circuit, and

a power management unit to turn off the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check unit indicates that there is no activity on the interconnect, and the power management unit to not turn off the receiver circuit after an electrical idle ordered set is processed by the pipeline and received by the power management unit if the interconnect activity check

unit indicates that there is activity of the interconnect.

13. The system of claim 12, wherein the pipeline includes a data extraction unit and a packet processing unit.

14. The system of claim 13, the receiver circuit including a pair of inputs to receive a pair of differential signals, the differential signals included as part of the interconnect.

15. The system of claim 14, the interconnect activity check unit to indicate that there is no activity on the interconnect if the differential pair of signals are at approximately a common mode voltage.

16. The system of claim 15, wherein the interconnect is a PCI Express interconnect.